CLAIMS

I claim:

1. A device, comprising:

a substrate with a first surface and a second surface, and having a plurality of conductors to electrically connect a plurality of pads on the first surface with a plurality of pads on the second surface;

a first integrated circuit die with a first surface and a second surface, and having a plurality of microelectronic devices;

a first plurality of conductive connection structures extending between the first surface of the first integrated circuit die and the first surface of the substrate, to electrically and structurally connect the substrate to the first integrated circuit die;

a second integrated circuit die with a first surface, and having a plurality of microelectronic devices;

a second plurality of conductive connection structures extending between the second surface of the first integrated circuit die and the first surface of the second integrated circuit die, to electrically and structurally connect the first and second integrated circuit dies; and

a sealing layer extending from the first surface of the substrate at least to the first surface of the second integrated circuit die, the sealing layer being around a perimeter of the first surface of the second integrated circuit die and a perimeter of the of the first surface of the first integrated circuit die to seal the second plurality of conductive connection structures from an environment surrounding the device.

2. The device of claim 1, wherein the sealing layer comprises an underfill material.

3. The device of claim 2, wherein the sealing layer substantially fills a volume between the first integrated circuit die and the second integrated circuit die and around the second plurality of conductive connection structures.

4. The device of claim 2, wherein the underfill material substantially fills a volume between the substrate and the first integrated circuit die and around the first plurality of conductive connection structures.

5. The device of claim 4, wherein the underfill material comprises filler particles having an average diameter greater than a distance between the first integrated circuit die and the second integrated circuit die.

6. The device of claim 1, wherein a first distance between the substrate and the first integrated circuit die is in a range from about 75 microns to about 100 microns, and a second distance between the first integrated circuit die and the second integrated circuit die is in a range from about 100 nanometers to about 200 nanometers.

7. The device of claim 1, further comprising a printed circuit board coupled to the substrate and memory coupled to the printed circuit board.

8. A device, comprising:

a substrate;

a first die above the substrate and spaced apart from the substrate by a first distance;

a first plurality of connectors extending from the substrate to the first die;

a second die above the first die and spaced apart from the first die by a second distance;

a second plurality of connectors extending from the first die to the second die; and

a sealing layer extending between the first die and the second die and substantially surrounding a perimeter of the first die and the second die, to substantially seal a volume between the first and second dies from a surrounding environment.

9. The device of claim 8, wherein the first distance is in a range from about 75 microns to about 100 microns, the second distance is in a range from about 100 nanometers to about 200 nanometers.

10. The device of 9, wherein the sealing layer substantially fills a volume between the first die and the second die and around the second plurality of connectors.

11. The device of claim 8, wherein the sealing layer comprises an underfill material.

12. The device of claim 11, wherein the underfill material extends from a top surface of the substrate at least to the bottom of the second die.

13. The device of claim 12, wherein the first distance is in a range from about 75 microns to about 100 microns, the second distance is in a range from about 100 nanometers to about 200 nanometers, and wherein the underfill material further comprises filler particles having an average diameter of about 1 micron or greater, the sealing layer also substantially filling a volume between the substrate and the first die and around the first plurality of connectors.

14. The device of claim 8, wherein the second plurality of connectors comprise a first set of copper connectors connected to the first die bonded to a second set of copper connectors connected to the second die, and wherein the first set of copper connectors extends a distance into the first die and the second set of copper connectors extends a distance into the second die.

15. A method, comprising:

forming a device comprising:

a substrate;

a first die above the substrate and spaced apart from the substrate by a first distance to form a first volume between the substrate and the first die, the first die having a plurality of microelectronic devices;

a first plurality of connectors extending from the substrate to the first die;

a second die above the first die and spaced apart from the first die by a second distance to form a second volume between the first die and the second die, the second die having a plurality of microelectronic devices;

a second plurality of connectors extending from the first die to the second die;

applying a layer of underfill material extending from the substrate to the second die to substantially seal the second volume between the first and second dies from a surrounding environment; and

curing the layer of underfill material after the underfill material has substantially filled the first volume between the first die and the substrate.

16. The method of claim 15, wherein forming the device comprises:

fabricating the first die, the fabricated first die having a first set of first portions of the second plurality of connectors;

fabricating the second die, the fabricated second die having a second set of second portions of the second plurality of connectors;

singulating the first die from a first wafer comprising a plurality of dies;

singulating the second die from a second wafer comprising a plurality of dies; and

bonding the first set of first portions to the second set of second portions to connect the first die to the second die.

17. The method of claim 16, wherein the layer of underfill material is applied after singulating the first and second dies from the first and second wafers.

18. The method of claim 15, wherein the layer of underfill material substantially fills a volume between the first integrated circuit die and the second integrated circuit die and around the second plurality of connectors.

19. The device of claim 15, wherein the layer of underfill material comprises filler particles having an average diameter greater than the second distance between the first die and the second die.

20. The device of claim 15, wherein the first distance between the substrate and the first die is in a range from about 75 microns to about 100 microns, and the second distance between the first die and the second die is in a range from about 100 nanometers to about 200 nanometers.